ISA design

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Type(2bit) | OP (2bit) | 3bit | 3bit | 8bit |  |
| Register mode | 00 | 00 (ADD)  01 (AND)  10 (SHR) | Range[000-101]  Select 6 register set R0-R5 | Range[000-101]  Select 6 register set R0-R5 | Unused bit |  |
|  | Type(2bit) | OP (2bit) | 3bit | 4bit | 7bit |  |
| Immediate mode | 01 | 00 (ADD)  01 (AND)  10 (SHR) | Range[000-101]  Select 6 register set R0-R5 | Range[000-101]  Select 6 register set R0-R5 | Unused bit |  |
|  | Type(2bit) | OP (2bit) | 4bit | 10bit |  |  |
| Branching mode | 10 | 00 (JMP)  01(JE) | 4bit RAM address line | Unused bit |  |  |
|  | | | | | | |

Control unit

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | REG\_EN | IMM\_sel | ZF | JMP\_sel |  |  |  |
| Register mode | 1 | 0 | 0 | 0 |  |  |  |
| Immediate mode | 1 | 1 | 0 | 0 |  |  |  |
| JMP | 0 | 0 | X | 1 |  |  |  |
| JE | 0 | 0 | 1 | 1 |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |